IEEE1394 AND IECG1883 PACKET FORMATS

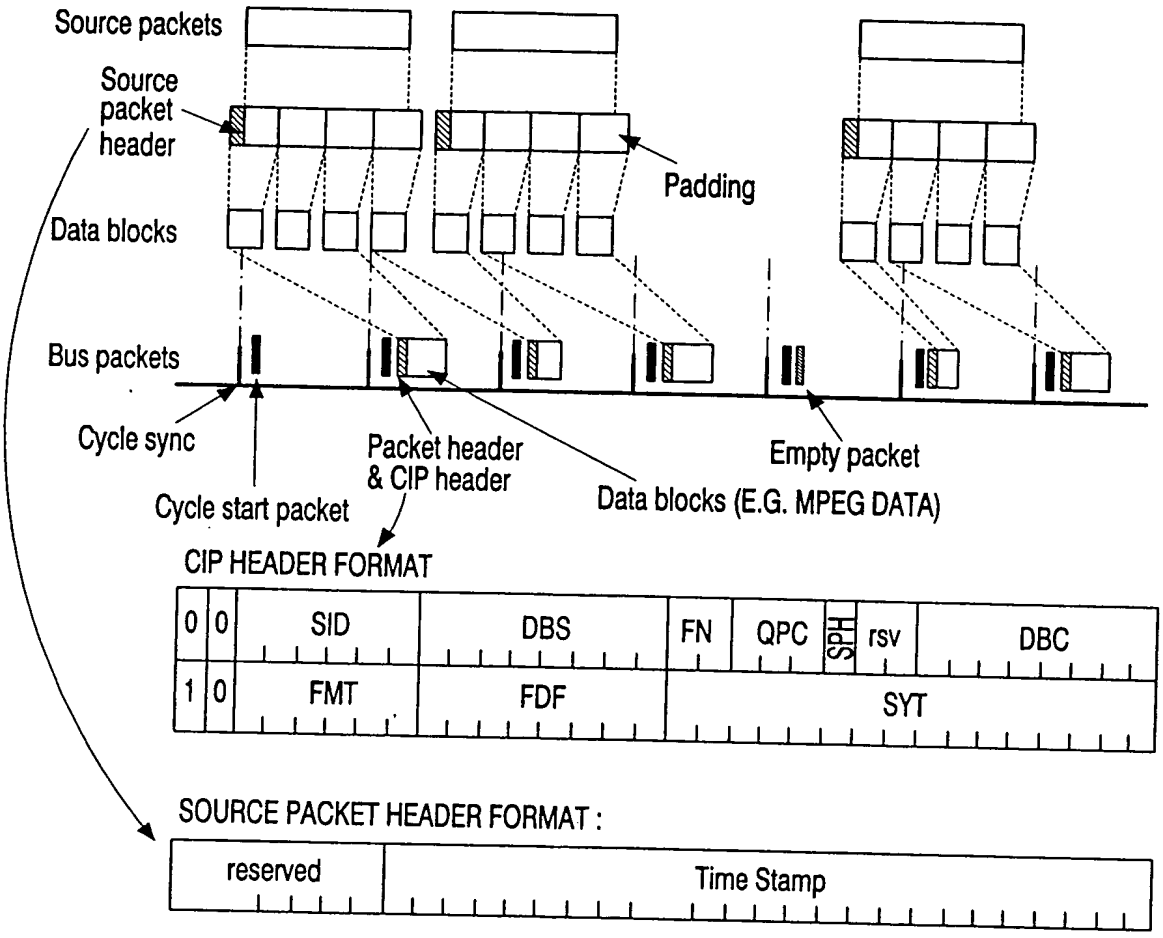

FIG. 1

CYCLE TIME REGISTER FORMAT

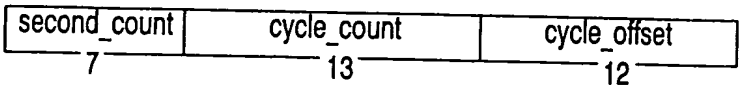

FIG. 2

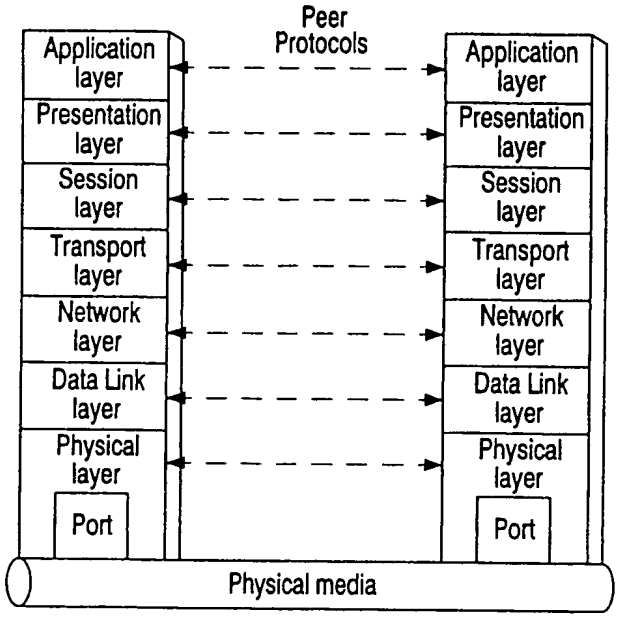
Peer
Protocols
Application layer
Presentation layer
Session layer
Transport layer
Network layer
Data Link layer
Physical layer
Port
Application layer
Presentation layer
Session layer
Transport layer
Network layer
Data Link layer
Physical layer
Port
Physical media

FIG. 3

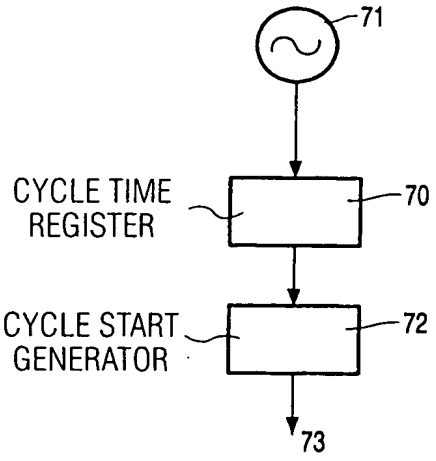
71
CYCLE TIME REGISTER
70
CYCLE START GENERATOR
72
73

FIG. 7

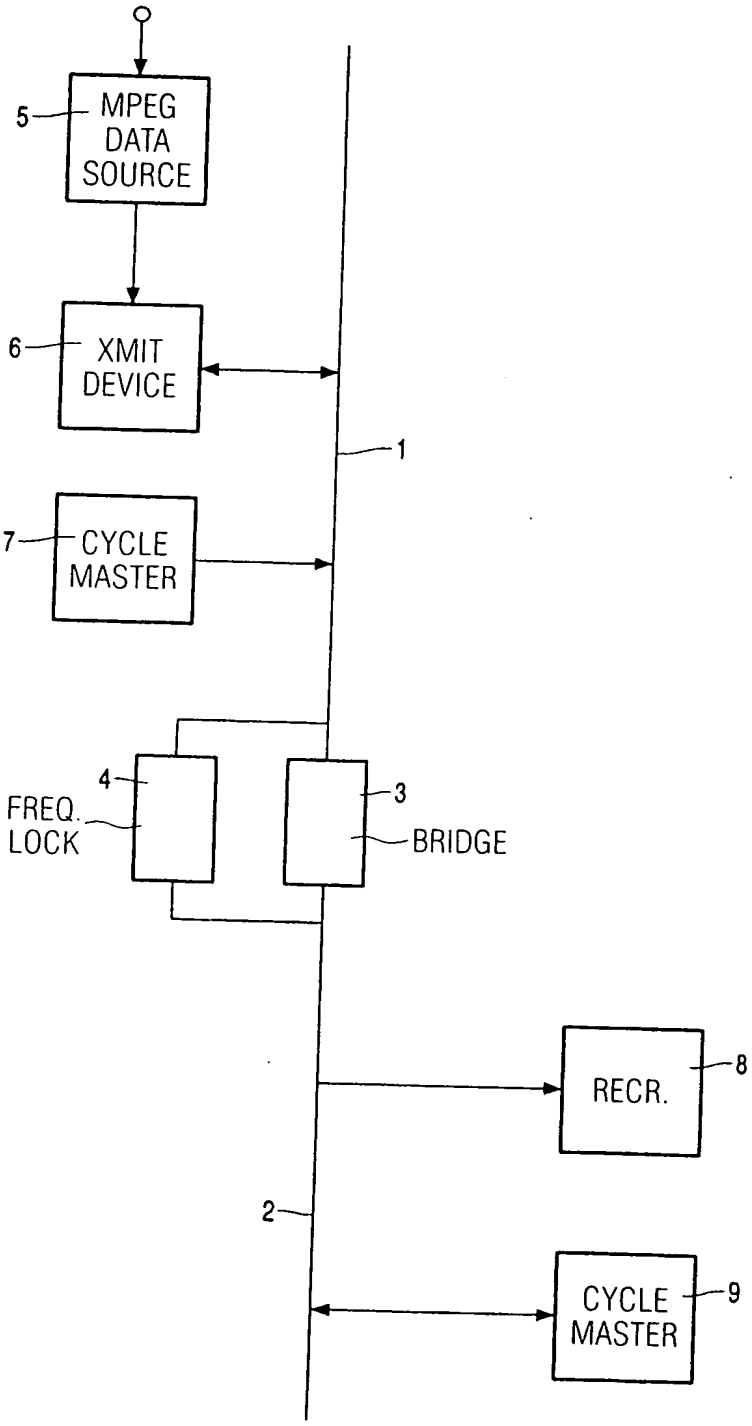
5
MPEG DATA SOURCE
6
XMIT DEVICE
1
7
CYCLE MASTER
4
FREQ. LOCK
3
BRIDGE
RECR.
8
2
CYCLE MASTER
9

FIG. 4

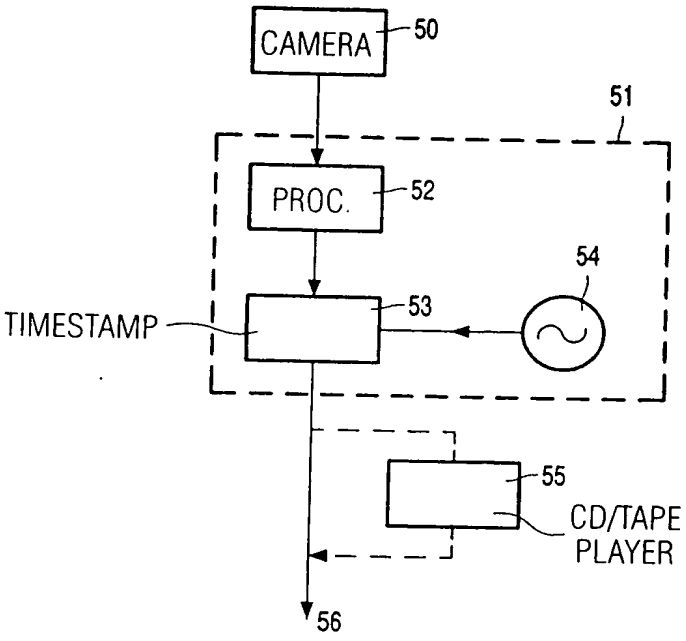
CAMERA
50
51
PROC.
52
54
TIMESTAMP
53
55
CD/TAPE
PLAYER
56

FIG. 5

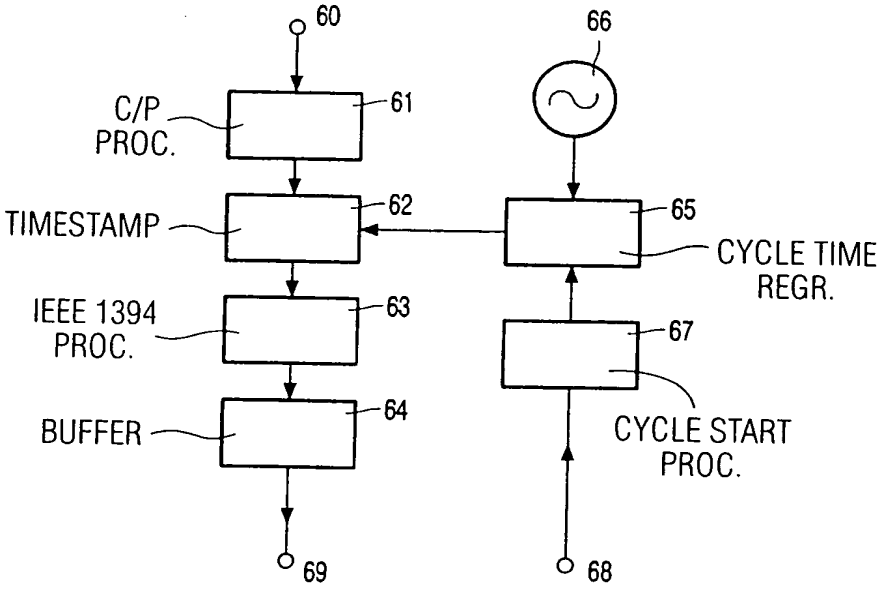
60
66
C/P
PROC.
61
TIMESTAMP
62
65
CYCLE TIME
REGR.
IEEE 1394
PROC.
63
67
BUFFER
64
CYCLE START
PROC.
69
68

FIG. 6

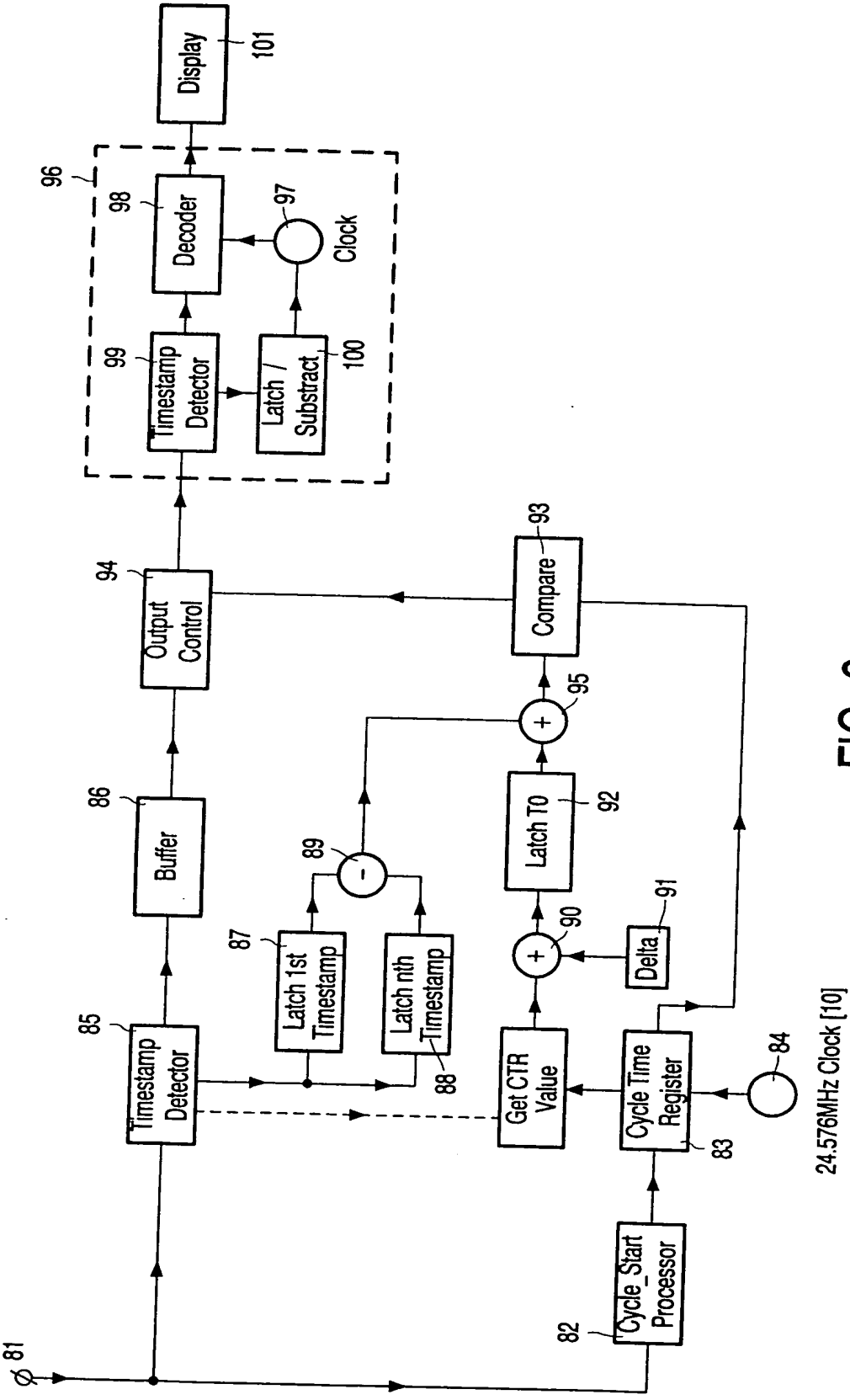
Display
101
96
98
Decoder
97
Clock
99
Timestamp Detector
Latch / Substract
100
94
Output Control
93
Compare
95
86
Buffer
89
Latch T0
92
87
Latch 1st Timestamp
Latch nth Timestamp
88
90
Delta
91
85
Timestamp Detector
Get CTR Value
Cycle Time Register
84
83
82
Cycle_Start Processor
81
24.576MHz Clock [10]

FIG. 8